

REMARKS

In the Official Action mailed on **30 June 2006**, the Examiner reviewed claims 1-4, 6-14, and 16-21. Claims 1-21 were rejected under 35 U.S.C. §102(b) as being anticipated by Chopra et al. (USPN 6,412,043 hereinafter “Chopra”).

Rejections under 35 U.S.C. §102(b)

Independent claims 1, 11, and 21 were rejected as being anticipated by Chopra. Applicant respectfully points out that Chopra teaches a method for improving a memory management unit (MMU) and cache memory (see Chopra, Title). This method involves widening the permission for a memory access by updating permission information for a particular entry in a virtual cache memory based on permission information for a corresponding entry in a translation lookaside buffer (TLB) (see Chopra, Abstract, and see Chopra, col. 42, lines 28-34).

In contrast, the present invention teaches a method for supporting read-only objects within an object-addressed memory hierarchy (see Title, and see page 9, paragraph [0038] of the instant application). Note that current object-addressed memory hierarchies do not support read-only copies of an object. The present invention teaches interposing a translator between cache and main memory (see FIG. 1, and see page 7, paragraph [0029], lines 7-8 of the instant application). This translator converts an object address into a corresponding physical address and a request to access an object into a request for the corresponding physical address (see page 9, paragraph [0029], lines 8-10, and see page 9, paragraph [0031], lines 21-23 of the instant application). Note that the translator is **not equivalent to a TLB**, which translates virtual addresses into physical addresses for non-object references (see page 6, paragraph [0023] of the instant application).

The present invention is advantageous because it allows read-only copies of an object to reside on multiple hosts (see page 2, paragraph [0003], lines 11-12 of the instant application). This provides significant performance advantages because it enables each host to access a read-only copy of the object in its local cache (see page 2, paragraph [0003], lines 13-14 of the instant application). Furthermore, an object-addressed memory hierarchy provides significant performance advantages over conventional memory hierarchies, which suffer from high levels of paging activity when executing object-oriented applications.

There is nothing within Chopra that suggests a translator for converting an object identifier and offset into a corresponding physical address and converting a request to access an object into a request for the corresponding physical address.

Accordingly, Applicant has amended independent claims 1, 11, and 21 to clarify that the translator converts an object identifier and offset into a corresponding physical address and converting a request to access an object into a request for the corresponding physical address. These amendments find support in paragraph [0029], and in paragraph [0031] of the instant application.

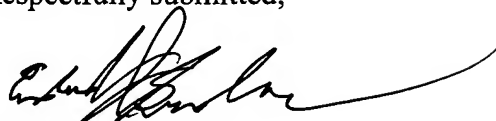
Hence, Applicant respectfully submits that independent claims 1, 11, and 21 as presently amended are in condition for allowance. Applicant also submits that claims 2-4, and 6-10, which depend upon claim 1, and claims 12-14, and 16-20, which depend upon claim 11, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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